synchronization in accordance with the TS 101 191 standard, [characterized in that it comprises] comprising:

N transmitters (12, 14) or transmission channels operating respectively at N different frequencies F1 to FN, each transmitter receiving a same digital signal to send in the form of packets in accordance with the MPEG2-TS standard,

N receivers (22R, 24R) or receiving channels operating respectively at N frequencies F1 to FN, each receiver supplying a succession of packets in accordance with the MPEG2-TS standard,

N error detection devices (22E, 24E) for detecting errors in the packets supplied by each receiver,

N synchronization devices (22S, 24S) for synchronizing the packets supplied by each receiver, and

a device for selecting one packet among the N available packets that does not contain an error or, failing that, a packet that corresponds to the lowest error rate.

2. (amended) System according to claim 1, [characterized in that it comprises] including N transmission antennas located at different positions and each receiving an output signal from one of the N transmitters.

3. (amended) System according to claim 1 [or 2, characterized in that it further comprises:]

including one to P receiving antennas which are located at different positions,

a device for combining signals received by the antennas to supply a combined signal, and

a device for distributing the combined signal among the N receivers.

4. (amended) System according to [any one of claims] claim 1 [to 3], [characterized in that it comprises] including per transmission channel:

a device (12D, 14D) for time shifting (T1 to TN) a digital signal received by each transmitter, the time shift (T1, T2) being different for each transmission channel, and

per receiving channel:

a device (22S, 24S) for timewise realigning digital signals supplied by the N receivers.

5. (amended) System according to claim 4, [characterized in that the] wherein said time shifting device (12D, 14D) comprises a buffer memory in which the digital signals are stored at an instant "t", said digital signals being read at instants (t + Ti) for signals applied to the transmitter of rank i among N.

6. (amended) System according to claim 4 [or 5, characterized in that the] wherein said timewise realignment device comprises, per receiver:

a circuit (22A, 24A) for detecting the start of each megaframe,

a buffer memory (22M, 24M) in which the packets are stored, beginning from the detection of the start of each megaframe, each packet having associated therewith an error information supplied by the error detection device, and

a circuit (20) for selecting one of the buffer memories so as to select a packet containing no error or, failing that, a packet corresponding to the receiving channel having the lowest error rate.

7. (amended) System according to claim 6, [characterized in that the] wherein said circuit for detecting the start of each megaframe comprises:

means for reading in a packet a pointer indicating the start of the following megaframe, and

means for adding in the first octet (byte) of the megaframe a ninth bit (D9) indicating the start of said megaframe.

8. (amended) System according to [any one of claims] claim 1 [to 7, characterized in that the] wherein said error detection device comprises:

means for detecting the error indicator in each packet, and

means for adding a ninth bit (D9) in the last octet of a packet preceding all error-containing packets, said ninth bit constituting the error indicator of the following packet.